**Digital Electronics Assignment march 2023**

**Question 1**

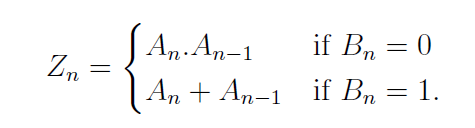
Consider the Boolean function below:

ab′ + b′c + a′bc

1. Use a 3 × 8 decoder plus whatever logic gates are needed to implement this function. [6]
2. Use an 8-input multiplexer to implement this function. [6]
3. Use a multiplexer and additional logic, including possibly exclusive-or gates, to implement this function by performing a Shannon expansion with respect to a (use a as the multiplexer control input). *Hint: it might be easier to eyeball a truth table than to do this by algebraic manipulation.* [8]

**Question 2**

1. With the aid of block and example state diagrams, describe the main features of Moore and Mealy implementations of finite state machines. [6]
2. A finite state machine (FSM) takes two inputs, A and B, and generates one output, Z. The output at cycle n, Zn, is



1. Determine the state transition table and the state diagram for a Mealy implementation of this FSM where the single D-type flip-flop state register has input A at its D-input. [5]
2. Write down the Boolean functions for the next state and output combinational logic for the FSM. [2]
3. Show how the FSM could be implemented using a 2:1 Multiplexor and some additional 2-input combinational logic gates. [2]
4. Show how the FSM could be modified to eliminate the asynchronous changes on the output Z in response to inputs A and B. [1]
5. An FSM may be implemented using a generic logic array (GLA) device or a generic array logic (GAL) device. With the aid of diagrams, compare and contrast the architecture of GLA and GAL devices, specially identifying the advantages and disadvantages of each device structure. [4]

**Question 3**

1. i. Give a labelled diagram of a JK flip flop. [2]

ii. With the aid of a truth table, describe the operation of this flip flop. [5]

1. An asynchronous counter goes through a counting cycle represented by a sequence of binary states as: 000,001,010,011,100,101,110,111,000 etc.

i. Deduce a truth table that summarises the counting operation of this digital

counter. [4]

ii. Determine the number of required flip flops in order to achieve the above

counting cycle. [4]

iii. Hence design a sequential logic circuit of this digital counter. [5]

**Question 4**

1. Consider a 4-input Boolean function that outputs a binary 1 whenever an odd number of its inputs are binary 1.
2. Using Boolean logic or otherwise, show how the above function can be implemented using only 2-input XOR gates. [4]
3. Show how the above function may alternatively be implemented using one 4-input decoder, and a minimum number of 4-input NOR and 4-input NAND gates. [3]
4. Consider the following Boolean expression 
5. Show that F can be represented by the following Product of Sums (POS) form  [3]
6. Show how F can be implemented in a 2-level form using OR gates followed by an AND gate. Remember to indicate any NOT gates required, since only uncomplemented input variables are available. [2]
7. Consider your implementation in part b. ii
8. Assume that the gates have finite propagation delay. Describe in detail what happens at the output F when the inputs {A, B, C, D} change from {1, 1, 0, 1} to {1, 1, 1, 1}. [4]
9. Using a Karnaugh map or otherwise, determine the other single input variable change that will give rise to a similar problem to that observed in part (c)(i ). [2]
10. Using a Karnaugh map or otherwise, determine a modified POS expression
11. for F that will eliminate the problems observed in parts (c)(i ) and (c)(ii ) [2]

**Question 5**

A lock has five buttons and a knob used to open the lock when the five buttons have been pressed in the correct sequence. Whenever the knob is turned, successfully or not, the state of the lock is reset. The correct sequence is hardwired into the control logic of the lock.

a. Describe the inputs and outputs for a logic circuit which can be used to control the lock.[5]

b. Draw a state diagram for the logic circuit. [10]

c. Derive equations for the logic system using J-K flip- flops to hold state variables. Do not minimize the equations. [5]